CLAIMS:

1. An electronic circuit comprising
- components that operate asynchronously of one another;
- an interface element, the interface element having an output and at least two inputs, each input coupled to a respective one of the components, the interface element supplying a logic output signal that is a logic function of signals at the inputs, dependent on the relative timing of the signals at the inputs;
- a delay element coupled to cause a relative delay between the times after which signals at the inputs affect the interface element;
- a control circuit for selectively activating the relative delay caused by the delay element prior to sampling an output signal of the interface element.

2. An electronic circuit according to Claim 1 comprising
- a test signal source coupled to the interface element;
- the control circuit being a test control circuit for switching the electronic circuit between a normal operating mode and the test mode, so that the signals at the inputs become affected by test signals from the test signal source during the test mode, the test control circuit activating said relative delay in the test mode and keeping the relative delay deactivated in the normal operating mode.

3. An electronic circuit according to Claim 1, wherein the interface element has enabling inputs, each for enabling signals from a respective one of the inputs, the control circuit having an activation output for supplying a deactivation signal followed by an activation signal during operation, the activation output being coupled to the enabling inputs, at least one of the enabling inputs via the delay element, so that the delay element causes a difference between the time intervals after which an activation signal from the activation output reaches different ones of the enabling inputs.

4. An electronic circuit according to Claim 3, wherein the interface element comprises a pair of cross-coupled logic gates, at least one of the logic gates comprising a

logic section and power supply interruption elements in series between an output of the at least one of the logic gates and power supply connections of the electronic circuit, the power supply interruption elements being arranged for switchably interrupting connections between an output of the at least one of the logic gates and both power supply connections of the electronic circuit, each input of the interface element being coupled to the logic section of a respective one of the logic gates, one of the disabling inputs being coupled to control inputs of the power supply connection element of the at least one of the logic gates.

5. An electronic circuit according to Claim 4, comprising
- a test control circuit for switching the electronic circuit between a normal operating mode and the test mode, the test control circuit activating said relative delay in the test mode and deactivating the relative delay in the normal operating mode,
- a scan chain for shifting test patterns in and/or out of the electronic circuit, the test patterns affecting input signals of the interface element in the test mode, wherein an output node of the at least one of the logic gates is incorporated as a dynamic storage node in the scan chain.

6. An electronic circuit according to Claim 2, comprising a scan chain for transporting test result patterns in the test mode, the scan chain being coupled to the interface element for reading information that depends on the output signal of the interface element.

7. A method of testing an electronic circuit that comprises components that operate asynchronously of one another and an interface element, the interface element having an output and at least two inputs, each input coupled to a respective one of the components, the interface element supplying a logic output signal that is a logic function of signals at the inputs and dependent on the relative timing of the signals at the inputs, the method comprising
- switching the electronic circuit to a test mode;
- applying test input signals to the electronic circuit from a test signal source;
- causing a difference between the time intervals after which the test signal source affects different ones of the signals at the inputs, the test control circuit activating said difference in the test mode and keeping the difference deactivated in the normal operating mode.